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HARRY DIAMOND LABS ADELPHI MD
A LOW-POWER DIGITAL TIMER WITH POTENTIOMETER SETTING MECHANISM. (U)

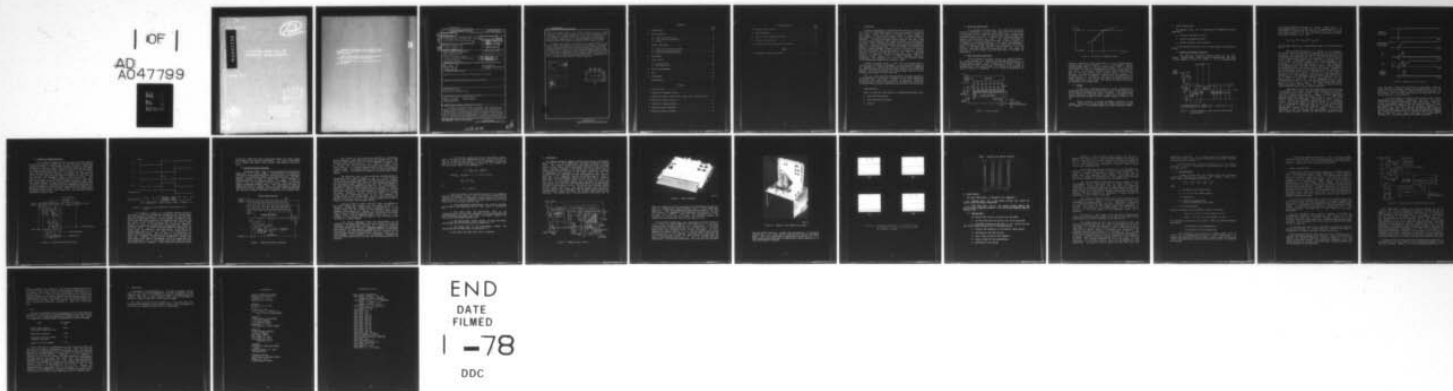
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cycle, the current drain of the circuit is 800 μ A at 5.5 V. After completion of the preset operation, the current consumption drops to 20 μ A at the reduced voltage of 3.6 V. This low operating power makes it possible to use this circuitry in a fuze with a fluidic power supply wherein a charged capacitor could bridge a temporary power loss during projectile flight through apogee.

Although the system is described with a potentiometer as the input device, the electronic part is not so limited. This preset scheme can be used whenever the digital output from the counter can be converted into a single-valued time-varying function commensurate with a constant or quasi-constant input quantity, which is a function of the desired time delay. During preset, the two quantities are compared while the counter counts at an accelerated rate, and when a predetermined condition is met, a feedback signal is generated that stops the preset operation.

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CONTENTS

	<u>Page</u>
1. INTRODUCTION	5
2. TIMER OPERATION	5
2.1 Reset and Arming Delay	6
2.2 Data Conversion and Preset	6
2.3 Timing	7
3. CIRCUIT DESCRIPTION	8
3.1 Power and Oscillator Circuits	8
3.2 Counter and Sequencing Logic	11
3.3 Analog-to-Digital Converter	13
4. PERFORMANCE	16
5. ERROR SOURCES	20
5.1 Setting Error	20
5.2 Time Base Error	22
6. DESIGN CONSIDERATIONS	23
7. COST	25
8. FUTURE WORK	26
DISTRIBUTION	27

FIGURES

1 Preset circuit	6
2 Voltages at comparator inputs	7
3 Voltage regulator, reset circuit, power switch, and oscillator .	8
4 Waveforms in reset circuit	10
5 Counter and sequencing logic	11
6 Sequencing logic waveforms	12
7 Analog-to-digital converter	13

FIGURES (Cont'd)		<u>Page</u>
8	Complete timer circuit	16
9	Timer breadboard	17
10	Complete timer demonstration model	18
11	Signals at power turnon	19
12	Planned timer using universal gate array	24

TABLE

I	Measured and Computed Timeouts	20
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1. INTRODUCTION

A general requirement for safety-and-arming devices is that a set of at least two independent conditions has to be satisfied in order to arm a round. Usually, the presence of setback and spin is sensed for this purpose. In the case of a mortar round or rocket where no appreciable spin exists, another quantity has to provide the second signature. A fluidic power supply used to power an electronic fuze not only converts mechanical into electrical energy, but also supplies the second signal required for arming, since a continuous electrical output is a positive indication that an airspeed is maintained that exceeds a certain minimum value. On the other hand, this necessity to maintain a certain minimum airspeed causes a possible loss of power when the round passes through the apogee of its trajectory. The only available source of electrical power during this time is the charge stored on a capacitor. Therefore, an electronic timer capable of operation through apogee has to exhibit extremely low power consumption. This requirement can best be met by a digital circuit using complementary symmetry MOS technology (CMOS).

A widely used method to set a time fuze is to rotate a part of the nose cone by an angle corresponding to the desired time delay or its complement. To achieve low power consumption without abandoning this familiar method of setting time fuzes, a timer was designed that combines a digital CMOS circuit with a potentiometer type of setting mechanism that rotates with the nose cone.

After the round has been fired and armed, the wiper position of the potentiometer is sampled and converted to its binary equivalent. At the same time, the timer is preset to this value. During the following timing operation, the counter is incremented at a rate that is derived from a crystal controlled oscillator until overflow occurs.

2. TIMER OPERATION

There are basically three phases in a complete operational cycle:

- a. Reset and arming delay
- b. Data conversion and preset
- c. Timing

2.1 Reset and Arming Delay

It is assumed in the discussion that follows that the supply voltage is generated by a fluidic power supply driven by the flow of air resulting directly from the flight of the round. A reset signal is generated when the supply voltage exceeds a certain minimum level indicating that the round is in motion. The reset pulse resets all counters and flip-flops in the timer. This action establishes a configuration in which the counter (described in detail in sect. 2.3) is counting at its normal timing rate. The number corresponding to the arming delay is decoded, and when the counter reads this state, a signal is generated that indicates that the motion of the round persisted from reset through the arming delay time. This signal can therefore be used for arming, and at the same time it initiates the preset phase.

2.2 Data Conversion and Preset

A block diagram of the basic circuit is shown in figure 1. The counter outputs are connected through buffer amplifiers to a resistor ladder network. If the counter is reset and then counts up, an ascending staircase voltage is generated at point A (fig. 2) starting from 0. The rate of change of V_A depends on the frequency at which the counter is incremented. In the initial configuration, the

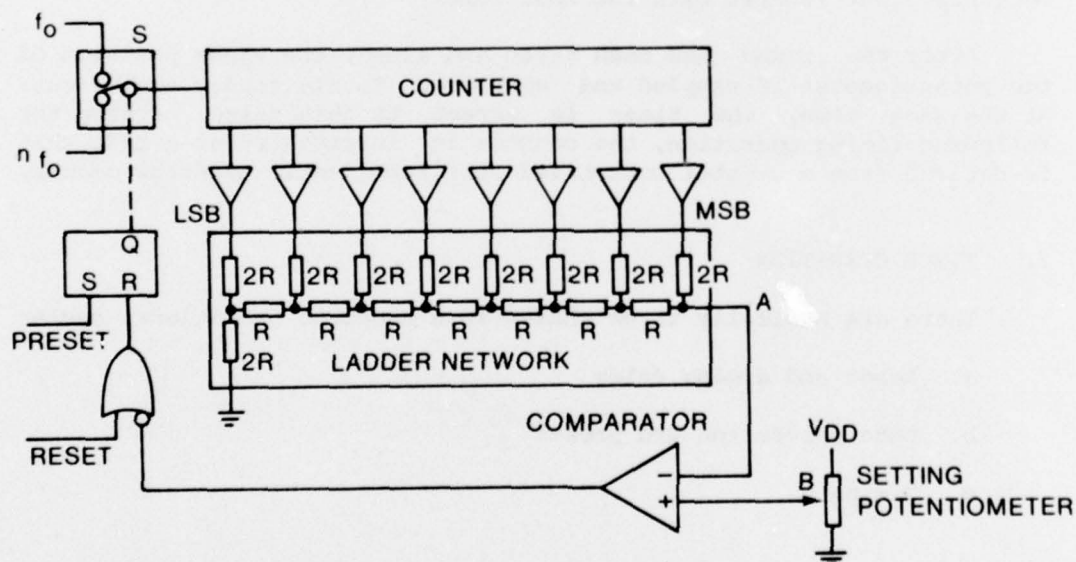


Figure 1. Preset circuit.

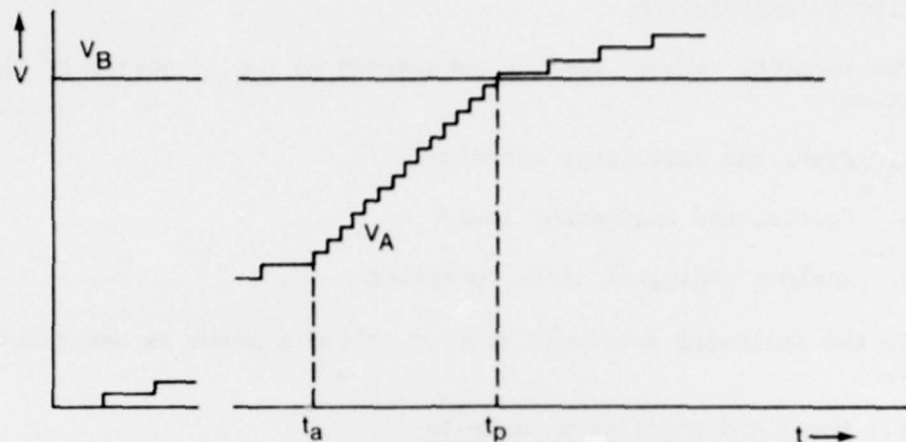


Figure 2. Voltages at comparator inputs.

counter is counting at (slow) timing rate f_0 , and V_A increases slowly. A preset signal changes the state of switch S , the counter counts at the accelerated rate, nf_0 , and V_A increases faster. When V_A crosses voltage level V_B , which is determined by the position of the potentiometer wiper, the resulting comparator output signal changes switch S back so that the counter counts again at rate f_0 . If the time necessary to preset the counter is less than one time increment $1/f_0$, no setting error is introduced. However, since the arming time has already expired at the time that the counter is preset, there is an offset equal to the arming time. This offset can easily be corrected by offsetting the indicator dial.

2.3 Timing

At the end of the preset operation, a logic configuration is established that selects the scaler output signal as the counting rate of the counter and enables the output circuitry. The output signal from the scaler has a frequency that is equal to the frequency of the crystal oscillator divided by a fixed integer (usually a power of 2 or 10).

Counter overflow is sensed by adding a flip-flop to the counter. This stage is triggered when the counter exceeds its maximum count capability. The overflow condition is used as an output signal.

3. CIRCUIT DESCRIPTION

The complete timer can be considered as the composite of three subsystems:

- a. Power and oscillator circuits
- b. Counter and sequencing logic
- c. Analog-to-digital (A/D) converter

In the following sections, each of these systems is described in detail.

3.1 Power and Oscillator Circuits

The power and oscillator circuits provide all the basic signals: supply voltage, reset signal at voltage turnon, and clock. A circuit diagram is shown in figure 3. Q1 is a depletion-mode

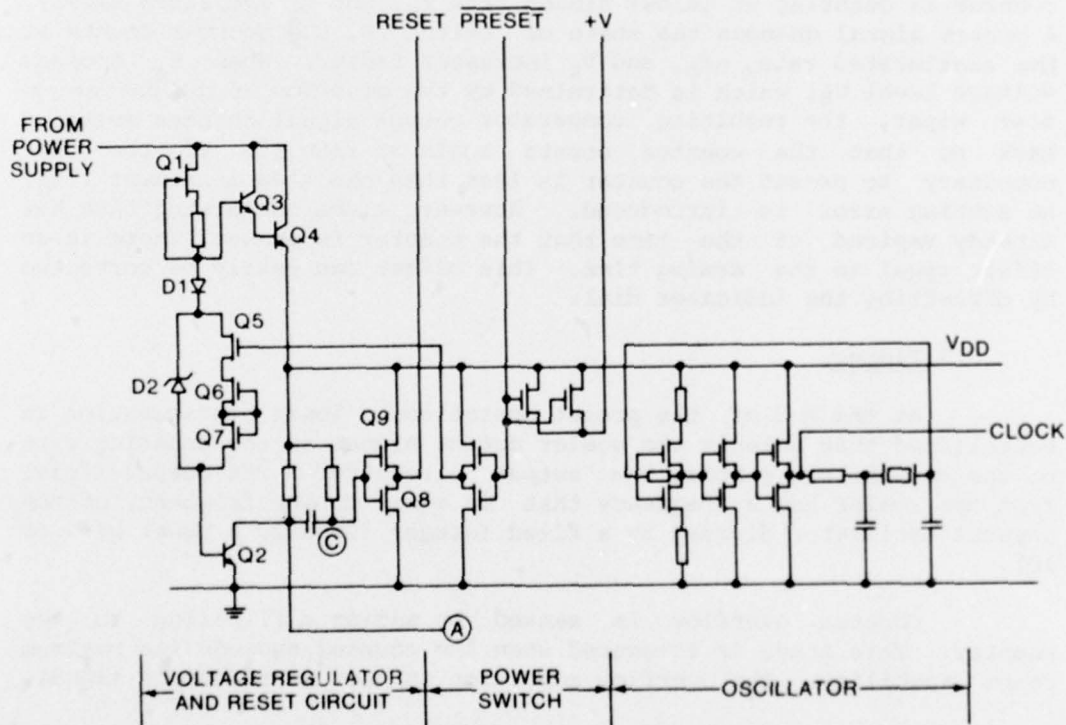


Figure 3. Voltage regulator, reset circuit, power switch, and oscillator.

field-effect transistor connected as a constant current source. In the breadboard model, the current was set to approximately 5 μ A. If Zener diode D2 is conducting, the potential at the base of Q3 is equal to the Zener voltage of D2 plus the voltage drop across D1 and the base emitter junction of Q2. Since

$$V_{D1} + V_{BE}(Q2) \approx V_{BE}(Q3) + V_{BE}(Q4),$$

the regulated voltage, V_{DD} , is approximately equal to the Zener voltage of D2.

When p-channel transistor Q5 is turned on, D2 is bypassed, the voltage across inverter Q6/Q7 is determined by the current passing through it, and the voltage is less than the Zener voltage of D2. D2 is therefore not conducting, and due to the high gain of Darlington Q3/Q4, the base current into Q3 can be neglected. It follows that V_{DD} in this case is approximately equal to the voltage necessary to sink in Q6 and Q7 the current supplied by Q1. In the breadboard, this voltage was 3.6 V and the Zener voltage was 5.5 V. Power consumption is considerably less at the lower voltage. However, startup problems were encountered with the oscillator at the low voltage. Furthermore, the minimum supply voltage for the amplifier used as the comparator in the A/D conversion circuit was 5 V. Therefore, the initial state of the circuit is chosen so that Q5 is off and the power switch is on, supplying +V to the comparator, resistor network, and potentiometer. At the completion of the preset operation, Q5 is turned on, and the power switch is turned off. In the breadboard circuit, power consumption was 0.8 mA at 5.5 V during arming delay and preset cycle and 20 μ A at 3.6 V during timing. The higher current drain during arming also ensures that the circuit is actually powered from the fluidic generator and not from a charged capacitor.

When power is turned on, all bistable circuits have to be set to a defined initial state. The pulse that accomplished this setting is generated in the reset circuit. Power is turned on at time t_0 (fig. 4). Constant current source Q1 charges the stray capacitance associated with the circuit; this charge results in a linear ramp voltage across the Zener diode. The voltage at points A and C (fig. 3) follows the reference voltage until D2 starts conducting current. This current turns on Q2, and the voltage at A and C drops to 0. The voltage at A stays 0 as long as Q2 is on; this condition can be used as a low-voltage indicator. The voltage at C rises exponentially towards V_{DD} , as shown in figure 4. The inverter consisting of Q8 and Q9 serves as a pulse shaper. As long as the input voltage and supply voltage are less than the threshold voltage

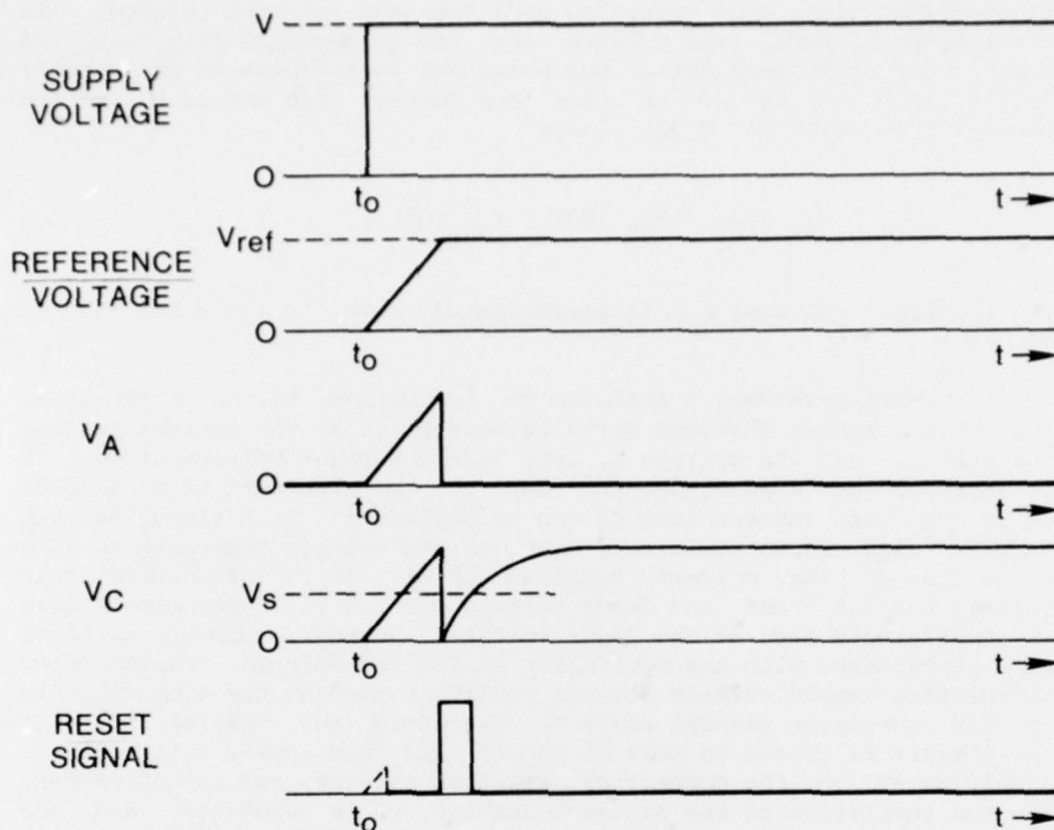


Figure 4. Waveforms in reset circuit.

of Q8, the output signal from the inverter is undetermined. When the input signal to the inverter exceeds the threshold voltage of Q8, the output is 0 until the voltage at C drops below switching voltage V_S of the inverter, and the reset signal goes to the high state and stays high as long as V_C is less than V_S .

In the oscillator, a 32,768-Hz watch crystal manufactured by Oscilloquartz SA, Neuchatel, Switzerland, was used. For future timers, it is planned to use crystals from STATEK Corp., Orange, CA, or some other domestic source as they may become available. At first, the oscillator was designed with one inverter according to RCA application note ICAN 6539. However, the startup time of such a circuit was rather long. Increasing the gain by using three inverters and starting the oscillator at 5.5-V supply voltage led to a startup time of less than 1 ms. After some delay, the voltage could be decreased to 3.6 V without affecting oscillator performance.

3.2 Counter and Sequencing Logic

The counter and sequencing logic provides the timing function by counting oscillator pulses and at the same time controls the sequence of events. A logic diagram is shown in figure 5. When power is turned on, the reset pulse resets both the scaler and the counter to the all-0 state and switches latches L1 and L2 to the reset state; this switching means that the L1 and L2 outputs are low. In this state, the power switch is turned on, output gate G4 is inhibited, and the 8-Hz output signal from the scaler is selected as the clock for the counter. The comparator output is high at this point. (For details, see sect. 3.3.) The counter counts at a rate of 8 Hz until the arming delay has passed (fig. 6) and the output of G1 goes high. This action switches L1, and G2 selects the accelerated counting rate of 8192 Hz, which is maintained until the comparator output goes low. Going low switches L2, which turns off the power switch, enables G4 to transmit an output signal, and again selects the 8-Hz clock signal. The counter counts at the slow timing rate until Q10 goes high and generates an output signal.

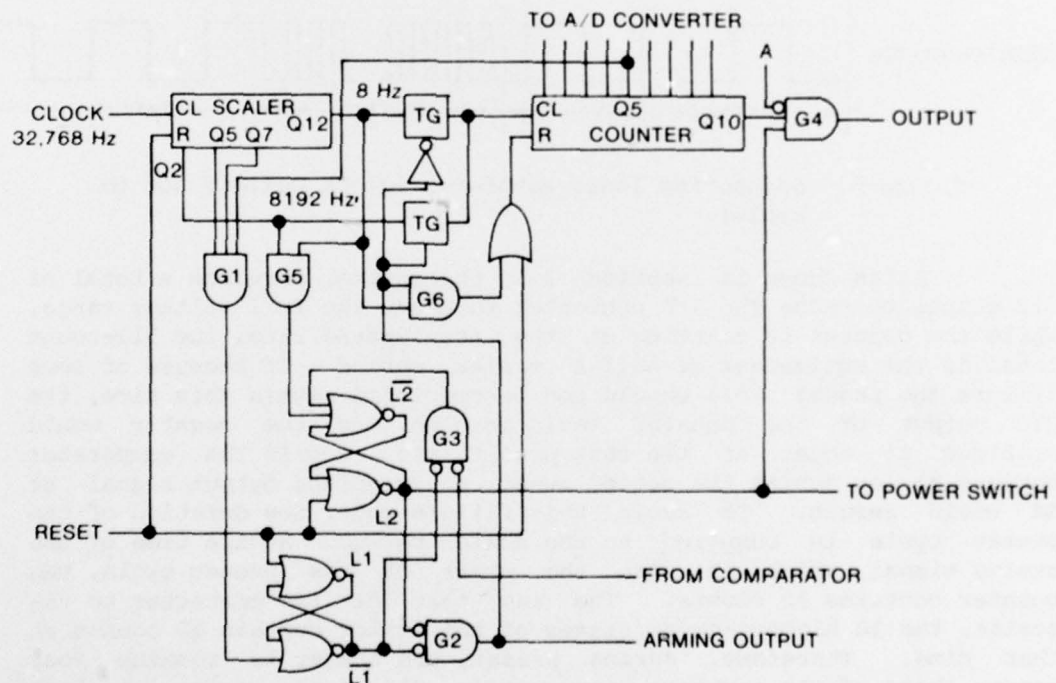


Figure 5. Counter and sequencing logic.

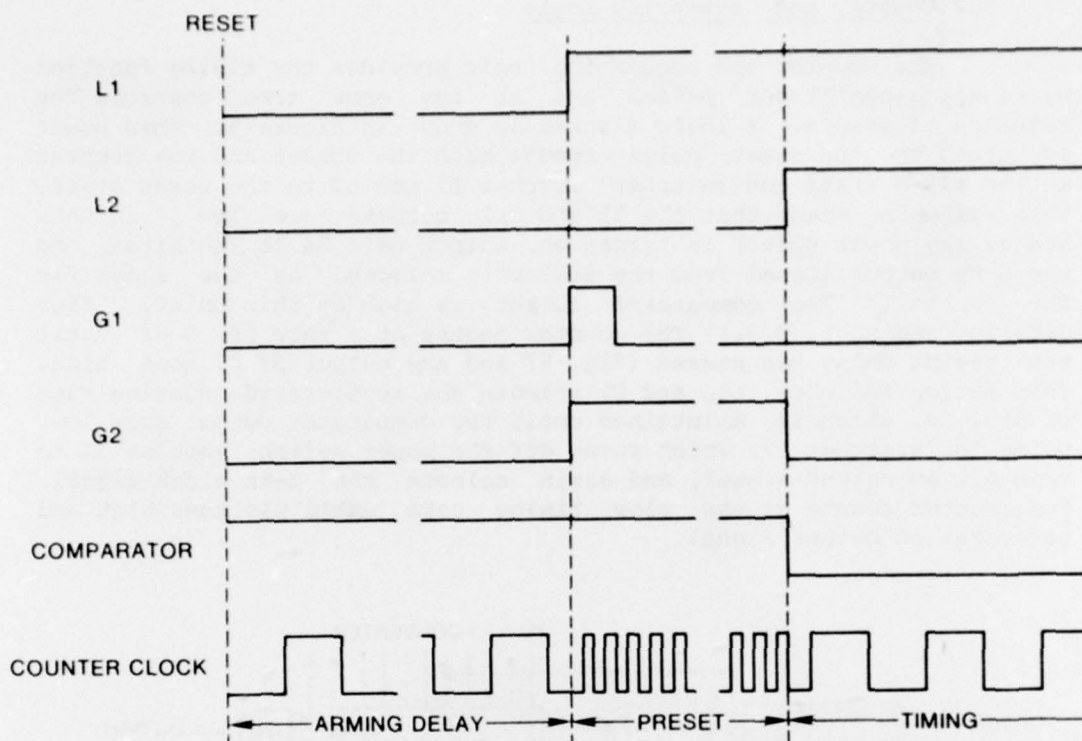


Figure 6. Sequencing logic waveforms (clock periods not to scale).

As is shown in section 3.3, the counter requires a total of 512 counts to cause the A/D converter to sweep the full voltage range. While the counter is counting at the accelerated rate, the 512-count total is the equivalent of half a scaler period. If because of some failure the preset cycle should not be completed within this time, the Q10 output of the counter would go high, and the counter would continue to count at the fast preset rate. Should the comparator outputs go low during the second sweep, an immediate output signal at G4 would result. To avoid this failure mode, the duration of the preset cycle is compared to the scaler period. At the time of the arming signal, which is also the start of the preset cycle, the counter contains 16 counts. The way that G1 is connected to the scaler, the 10 highest-order stages of the scaler contain 20 counts at that time. Therefore, during preset, the scaler is running four counts ahead of the counter; consequently, Q12 of the scaler goes high four counts before Q10 of the counter goes high. When Q12 of the scaler goes high, Q6 generates a reset pulse that resets the counter

to the all-0 state; and half a clock period later, L2 is set, putting the counter into the timing configuration. The timer is thus preset to its longest time, which is the required safe action in case of an error.

3.3 Analog-to-Digital Converter

The desired delay time is set by mechanically positioning a marked dial to the correct number. Simultaneously, this position is reflected by the voltage observed at the wiper contact of a potentiometer that is mechanically linked to the indicator scale. The timer, however, requires an input in digital form. This conversion is accomplished in the A/D converter circuit. A schematic is shown in figure 7. The A/D converter contains mostly linear circuits that require considerable standby power. Since this part of the timer is needed only during the preset cycle, its power supply is separated from the rest of the system by the power switch, which supplies power only during the interval from reset to completion of the preset cycle.

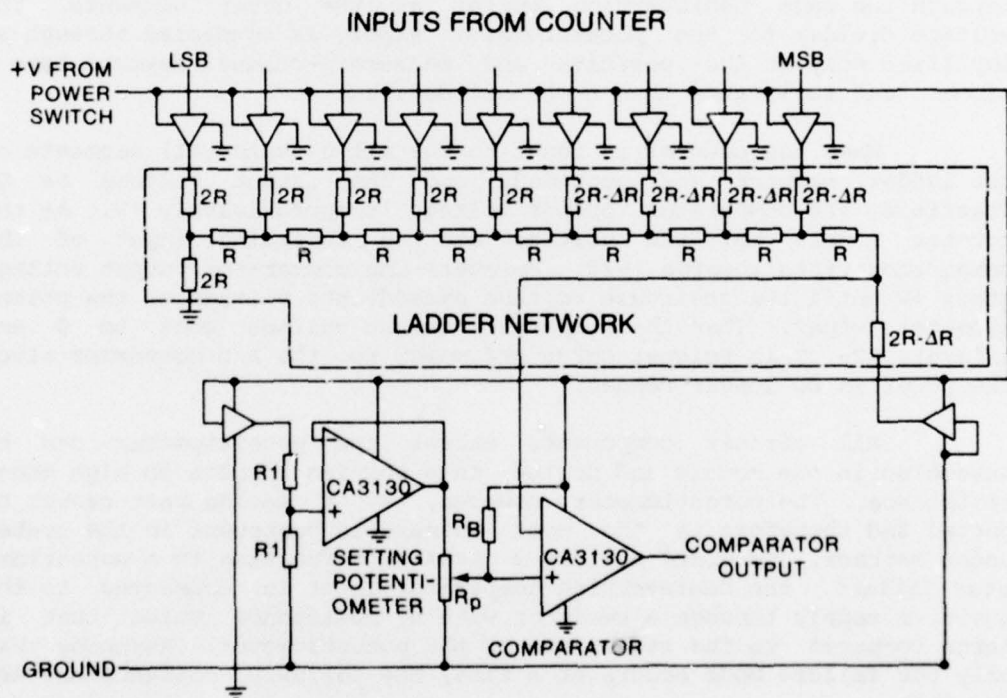


Figure 7. Analog-to-digital converter.

The outputs of the counter are connected to noninverting buffer amplifiers. These amplifiers connect the terminals of an $R/2R$ resistor ladder network to $+V$ or to ground depending on whether the corresponding bit in the counter is 1 or 0. When the counter counts up starting from the all-0 state, the voltage at the output of the ladder network is a staircase voltage starting from 0 and increasing in equal steps. The maximum number of steps is equal to the maximum number of counts. This voltage is compared to the potentiometer wiper contact.

The comparator used in this circuit was selected because it can operate from a supply voltage as low as 5 V, and its output voltage swing is directly compatible with CMOS logic levels. However, due to the limited common-mode range, the input voltage cannot exceed half the supply voltage. Therefore, the most significant segment of the ladder network is permanently grounded, and the potentiometer is operated at half the supply voltage, which is supplied by another operational amplifier in a voltage follower configuration. The five most significant bits of the ladder network are compensated for switch resistance. Therefore, the most significant segment is grounded through the same noninverting buffer as the other segments. The voltage divider for the potentiometer supply is connected through an amplifier only on the positive end because p-channel devices have a higher "on" resistance than n-channel devices.

When the counter is reset to the all-0 state, all segments of the ladder network are grounded, and the output voltage is 0. Therefore, the comparator output voltage is approximately $+V$. As the counter counts up, the voltage at the inverting input of the comparator rises towards $+V/2$. However, the comparator output voltage stays $+V$ until the staircase voltage exceeds the voltage at the potentiometer wiper. Then the comparator output voltage goes to 0 and triggers L2. This trigger turns off power to the A/D converter since the power is no longer needed.

All circuit components except the potentiometer can be assembled in one module and potted; this potting results in high shock resistance. The potentiometer, however, as a moving part cannot be potted and therefore is the most vulnerable component in the system under setback. To guard against a premature function in a potentiometer failure, the noninverting comparator input is connected to the positive supply through a resistor with a resistance value that is large compared to the resistance of the potentiometer. Assuming that only one failure mode occurs at a time, the following malfunctions are possible:

a. The positive supply lead to the potentiometer breaks: Power is supplied to the potentiometer through biasing resistor R_B (see fig. 7) and the wiper contact. If the potentiometer has resistance R_p and the fraction from wiper to ground is αR_p , voltage V' at the noninverting input to the comparator is

$$V' = \left[\alpha R_p / (\alpha R_p + R_B) \right] (+V) .$$

Since $R_B > 2R_p$ and $0 < \alpha < 1$, there is always

$$\alpha R_p + R_B > 2R_p$$

or

$$V' < \alpha (+V)/2 .$$

Since the voltage at the noninverting input of the comparator with the potentiometer intact would be $\alpha(+V)/2$, the voltage at the noninverting input of the comparator is always lower than it would be without failure. Thus, the comparator triggers earlier, and the timer times out at a time longer than set time.

b. The potentiometer breaks between the positive terminal and the wiper: This malfunction has the same effect as malfunction "a."

c. The wiper opens: The noninverting input of the comparator goes to $+V$, and the comparator is not yet triggered when the Q12 output of the scaler goes high. The counter is reset to the all-0 state, the longest possible time.

d. The potentiometer breaks between the wiper and ground: This malfunction has the same effect as malfunction "c."

e. The ground wire to the potentiometer breaks: This malfunction has the same effect as malfunction "c."

In all cases, the timer fails long, as required.

4. PERFORMANCE

The complete system as shown in figure 8 was built on a wire-stitch board (fig. 9) by using commercially available integrated circuits (IC's). The resistor network was a TRW type 5045 10-bit thin-film ladder, and the crystal was an Oscilloquartz SA watch crystal type 4VHC6 with a resonant frequency of 32,768 Hz. The circuit board can be plugged into a fixture that has all the necessary peripheral equipment to demonstrate the operation of the timer system (fig. 10). The following data were taken when the timer was plugged into this fixture, which uses a 9-V transistor battery as the power supply. Figure 11 shows some signals immediately after the power was turned on. There is some bounce of the switch contact for a little less than 1 ms (fig. 11a). In the regulated voltage, this bounce shows up as a notched step voltage (fig. 11b) due to the rectifying effect of the base emitter junction of the Darlington circuit. The contact bounce causes a series of reset pulses (fig. 11c). This series assures that the correct initial conditions are established when the supply voltage reaches its quiescent state. Figure 11(d) shows the startup phase of the crystal oscillator. The startup time of the oscillator is just under 1 ms. To

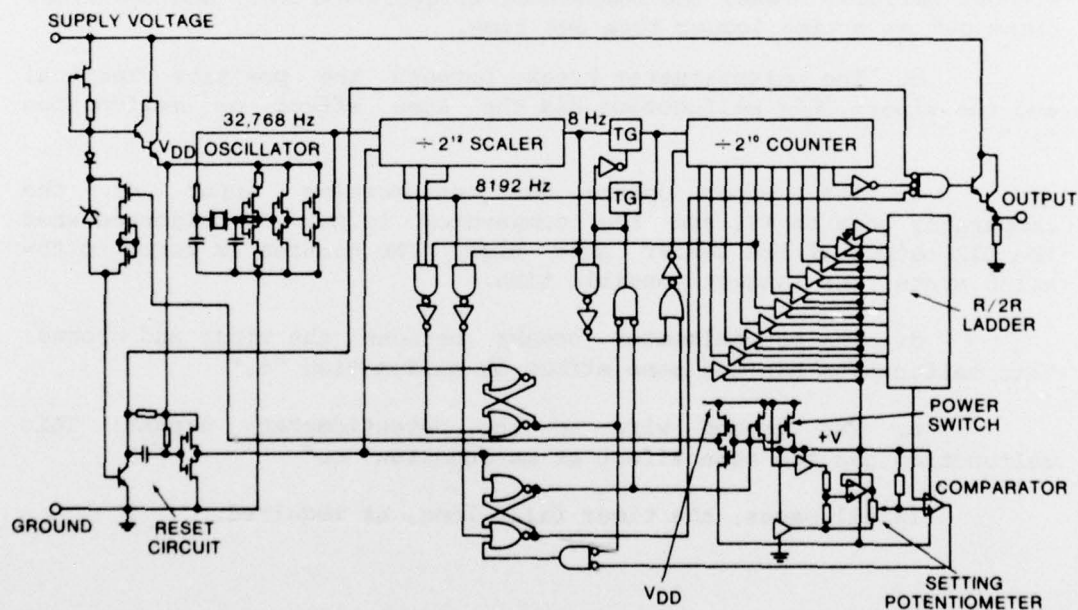
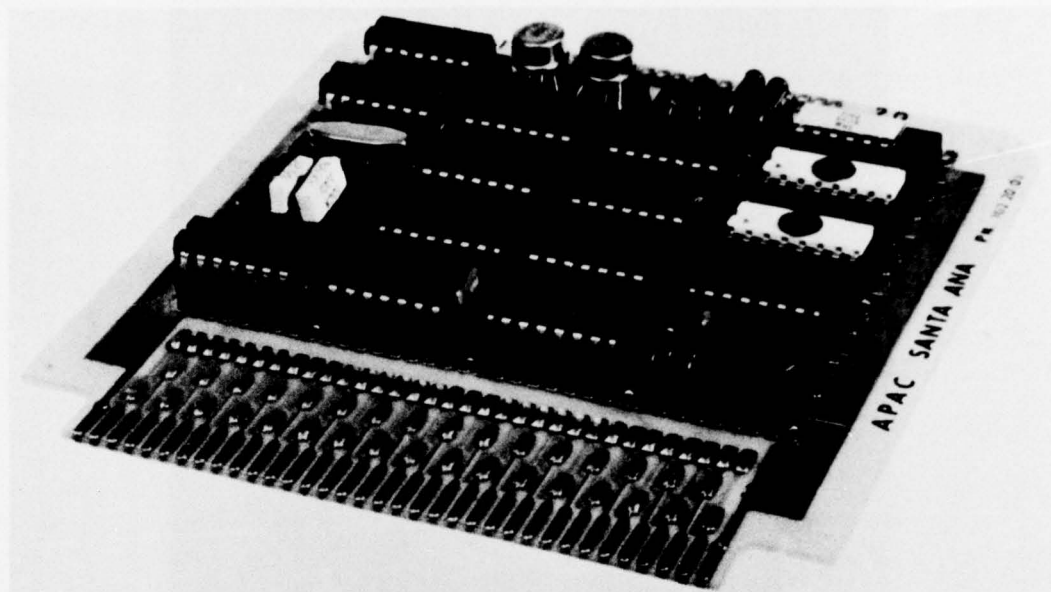


Figure 8. Complete timer circuit.

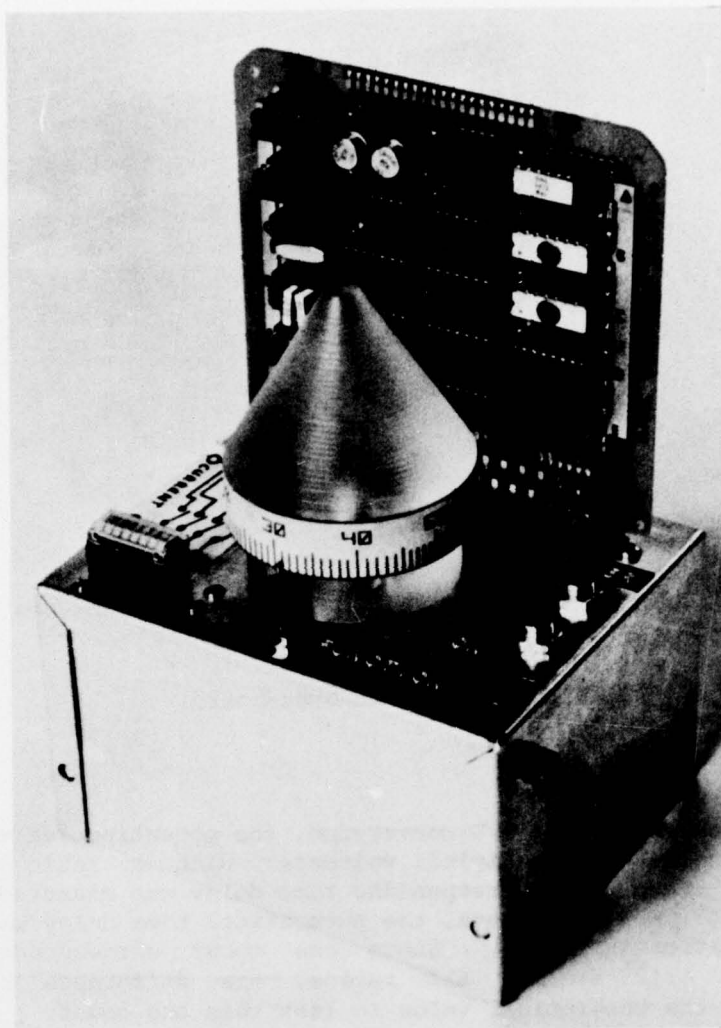


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Figure 9. Timer breadboard.

check the accuracy of the A/D conversion, the potentiometer was set to a ratio as indicated by a digital voltmeter with a ratio measurement capability. Then the corresponding time delay was measured for each ratio setting. For comparison, the theoretical time delay was computed for each ratio (table I). Since one count corresponds to a time increment of 0.125 s, for all ratios, the difference between the measured and the theoretical value is less than one count.

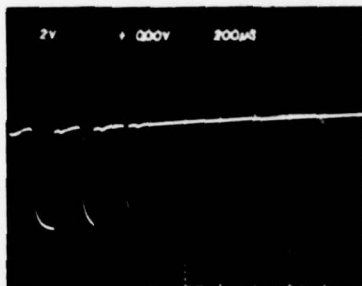
The regulated voltage during the arming delay and preset cycles is 5.5 V, and for the timing operation it is reduced to 3.6 V. The corresponding supply currents are 800 and 20 μ A, respectively. If the timer is operated from a charged capacitor, the operating time is 1.25 ms/V μ F during arming and 50 ms/V μ F during timing. For example, if a 20- μ F capacitor is charged initially to 15 V and the minimum supply voltage for the timer is 7 V, the capacitor can supply power to the timer for 8 s in the timing mode. During the arming delay, the same charge can keep the timer operating for only 0.2 s. Thus, to maintain the timer running for 2 s in the high-current mode, the power has to be delivered



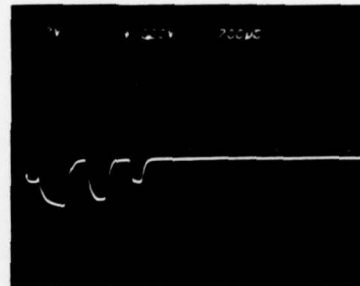
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Figure 10. Complete timer demonstration model.

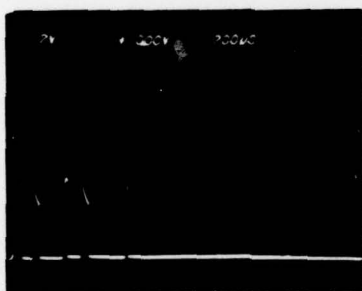
from the fluidic generator. If power from the generator is interrupted for more than 0.2 s, a reset pulse is generated that starts a new arming delay. This action shows that an arming signal at the end of a 2-s delay period during which power is supplied by a fluidic generator is a valid environmental signature.



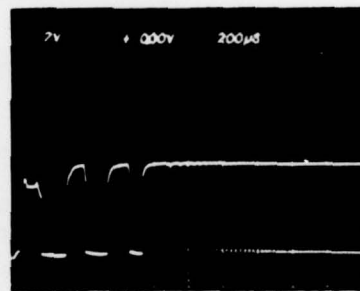
(a)



(b)



(c)



(d)

Figure 11. Signals at power turnon: (a) supply voltage, (b) regulated voltage, (c) reset signal, and (d) oscillator startup.

TABLE 1. MEASURED AND COMPUTED TIMEOUTS

Resistance ratio	Time measured (s)	Time computed ^a (s)	Time difference (s)
0.95	5.241	5.127	0.114
0.90	8.373	8.377	-0.004
0.85	11.504	11.502	0.002
0.80	14.759	14.752	0.007
0.75	18.015	18.002	0.013
0.70	21.143	21.127	0.016
0.65	24.397	24.377	0.020
0.60	27.529	27.502	0.027
0.55	30.785	30.752	0.033
0.50	34.038	34.002	0.036
0.45	37.169	37.127	0.042
0.40	40.423	40.377	0.046
0.35	43.554	43.502	0.052
0.30	46.684	46.752	0.068
0.25	49.938	50.002	0.064
0.20	53.193	53.127	0.066
0.15	56.324	56.377	0.053
0.10	59.577	59.502	0.075
0.05	62.709	62.752	0.043

^aThese values were obtained by simulating the conversion and timing cycles on a programmable calculator.

5. ERROR SOURCES

The total timing error is composed of two components:

a. Setting error, due to the limited accuracy with which the initial conditions can be established

b. Time base error, due to the finite startup time of the oscillator and a possible deviation of the oscillator frequency from its nominal value.

5.1 Setting Error

The factors that produce a setting error are these:

- a. Accuracy with which the setting ring can be positioned
- b. Discrepancy between the markings on the setting ring and the actual voltage divider ratio of the potentiometer
- c. Accuracy and resolution of the resistor ladder network
- d. Resistance of the CMOS switches
- e. Input offset voltage of the comparator
- f. Supply voltage for the potentiometer
- g. Resolution of the counter

Assuming a total nose-cone rotation angle of 300 deg and a maximum time range of 60 s yields turning increments of 5 deg/s. If there is a marking for each second, fractional settings can be estimated to 0.2 s. The resolution of the counter and resistance ladder is 0.125 s. The accuracy of most commercially available ladder networks is $\pm 1/2$ least significant bit.

The contribution from error sources b to f can be minimized by engraving the time markings after the timer has been assembled. The counter is stepped in increments of seconds. Then the nose cone is turned until the comparator output changes. At the same time, the position is marked on the setting ring. This process can be automated and is thus suitable for incorporation into an assembly line.

The voltage divider to generate the supply voltage for the potentiometer can be incorporated into the ladder network. This incorporation reduces the parts count and makes the temperature coefficient of the voltage divider and the ladder network the same. The output voltage of the potentiometer and the output voltage of the ladder network depend only on the ratio of resistors manufactured from the same material. The ratio change due to variations in supply voltage or temperature or due to aging is negligible.

The comparator used in the model has an input offset voltage of 8 mV typical and 15 mV maximum. At 5.5-V operating voltage, this corresponds to a maximum offset of 0.35 s. This offset is compensated at room temperature if the above described calibration procedure is followed. The change in input offset voltage with temperature is 10 $\mu\text{V}/^\circ\text{C}$. This would result in a maximum setting error of 0.016 s for a deviation of 70°C with respect to room temperature, which can be neglected.

The effect of the change in the CMOS switch resistance with temperature can be minimized by making the R value of the ladder network large compared to the "on" resistance of the CMOS devices.

The ladder network in the model has an R value of 50 k Ω . The five most significant bits are 150 Ω less to compensate for the switch resistance. The maximum "on" resistance of the n-channel device in the CMOS buffer is 105 Ω at -40°C and 190 Ω at +85°C. Therefore, the error caused by the n-channel device is reasonably well compensated. The p-channel transistor has a maximum "on" resistance of 670 Ω at room temperature, which causes an error of 4.5 mV in the most significant bit or an error in time of 0.104 s, which is compensated in the calibration procedure. The switch resistance changes to 570 Ω at -40°C and 800 Ω at +85°C. This change introduces an error with respect to room temperature of less than 0.025 s, which can be neglected in this application. The error in the next lower bit is half this value and

therefore not considered. In a custom circuit, the p-channel devices can be made bigger, or two or three transistors can be used in parallel and reduce the error further.

It follows that the initial value can be set to 0.2 s with an uncertainty of ± 0.125 s corresponding to the resolution of the counter and ladder network.

5.2 Time Base Error

As shown in figure 11(d), the startup time of the oscillator is less than 1 ms and can be neglected. The frequency change of a quartz crystal with temperature is given by

$$\Delta f/f_o = -\alpha(T - T_o)^2 + \alpha(T_r - T_o)^2,$$

where

f_o = frequency at room temperature,

$\alpha = 4 \times 10^{-8} \text{ } ^\circ\text{C}^{-2}$ for STATEK crystal,

T = temperature,

T_o = turning point temperature

$= -30^\circ\text{C}$ for STATEK SX or SV crystal,

T_r = room temperature.

Using the constants for the STATEK SX crystal, one obtains

$$\Delta f/f_o = 1.2 \times 10^{-4} \text{ or } 0.012 \text{ percent at } -30^\circ\text{C},$$

$$\Delta f/f_o = -2.8 \times 10^{-4} \text{ or } -0.028 \text{ percent at } +70^\circ\text{C}.$$

The calibration accuracy is ± 0.03 percent. Hence, the maximum frequency deviation is

+0.042 percent at low temperatures,

-0.058 percent at high temperatures.

This deviation would result in a maximum timing error of 0.025 s at low temperatures and -0.035 s at high temperatures if a maximum time setting of 60 s were assumed. These values are nearly one order of magnitude smaller than the positioning error and can therefore be neglected.

The crystal frequency change due to aging is quoted by STATEK as 10 ppm during the first year and less than twice this amount during 10 years. This is about one order of magnitude less than the frequency change with temperature and can therefore be neglected.

6. DESIGN CONSIDERATIONS

The main design goal was low power consumption to overcome possible loss of airspeed during passage through apogee which is most likely to occur in low-velocity mortar rounds. Associated with the low muzzle velocity are reduced acceleration forces. This reduction makes it possible to use the STATEK low-frequency crystal for the oscillator. According to the manufacturer, these crystals can be used in applications up to 10,000 g without design changes, only with tighter quality control, and there is a chance of improving the crystals for use at higher acceleration levels. For medium accuracy (2 to 3 percent) at high acceleration levels (up to 30,000 g), the crystal oscillator can be replaced by an RC oscillator. This replacement would not necessitate any design changes since the active part of the oscillator can be designed in such a way that it works with a crystal or an RC circuit as frequency determining element.

A crystal for a high-acceleration application would most likely have to be an AT cut with a special shock mount. The lowest frequency for which such a crystal can be manufactured is about 5 MHz. However, these crystals are considerably more expensive and need additional divider stages. A divider for this frequency will probably have to be of the silicon-on-sapphire (SOS) CMOS type to stay within the low power requirement.

The most economical way to obtain a working IC suitable for environmental testing is to implement all CMOS circuits on an RCA Universal Gate Array (UGA). This chip contains a matrix of p- and n-channel transistors and requires only a customized metallization mask. The UGA is also available in SOS technology for operation with higher oscillator frequency.

The combined CMOS and bipolar amplifiers are monolithic circuits. They can be integrated on a custom CMOS chip. However, they cannot be accommodated on currently available universal gate arrays.

After considering all the above facts, the most efficient way to continue this program appears to be to build a system with several IC packages and discrete components as shown in figure 12. If a high volume application warrants the additional development cost, the component count can be further reduced by using a genuine custom IC that can accommodate the two amplifiers.

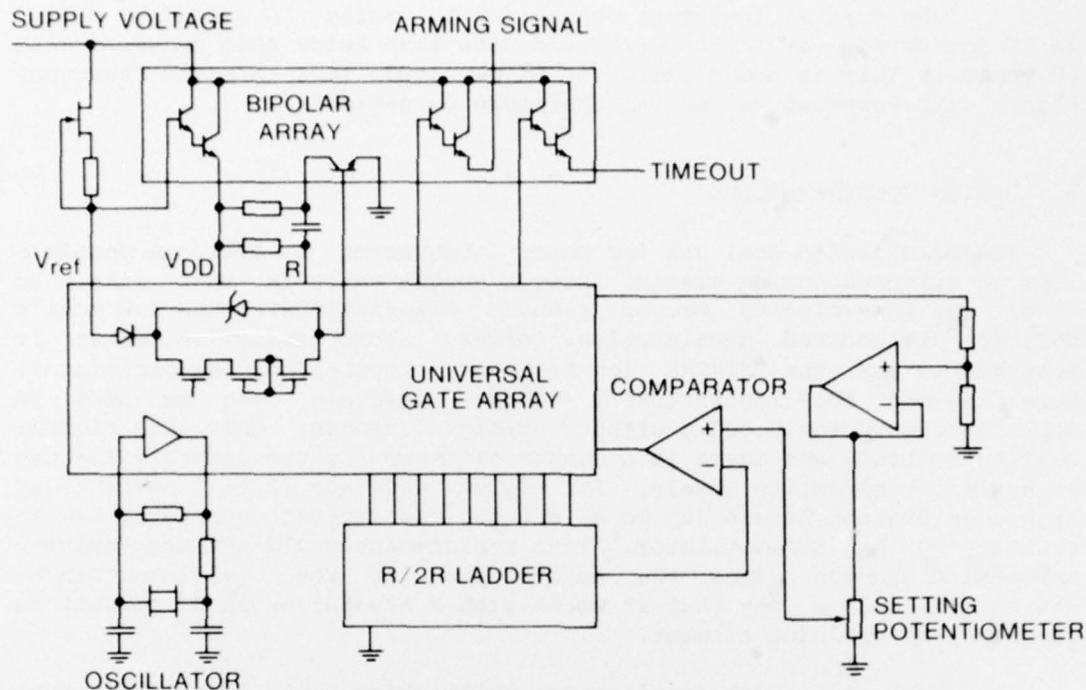


Figure 12. Planned timer using universal gate array.

Most commercially available R/2R resistor networks are of the thin-film type. The main advantages of thin-film networks are that, in general, they have a low temperature coefficient (± 5 to ± 25 ppm/ $^{\circ}\text{C}$), tight temperature coefficient tracking (± 1 to ± 5 ppm/ $^{\circ}\text{C}$), uniform aging, and the ability to be trimmed to very tight tolerances (as low as ± 0.01 percent absolute and ± 0.005 percent ratio). The resolution of most networks is 10 or 12 bits with an accuracy of $\pm 1/2$ least significant bit over the full specified temperature range. Thick-film networks are less expensive. However, generally they have a higher temperature coefficient and worse temperature coefficient tracking, and they cannot be adjusted as tightly as thin-film ladders. The range for thick-film temperature coefficients is ± 100 to ± 250 ppm/ $^{\circ}\text{C}$, and temperature coefficient tracking is in the range of ± 25 to ± 50 ppm/ $^{\circ}\text{C}$. Considering the accuracy with which the setting ring can be positioned, a ladder network with a resolution of nine bits, possibly even eight bits, and an accuracy of $1/2$ least significant bit should be sufficient.

If the scale of the setting ring can be calibrated together with its corresponding timer, the linearity of the setting potentiometer should not pose a problem. However, if a uniform turning-angle/set-time scale

factor is required, the linearity of the setting potentiometer has to be of the same order as the resolution of the resistor ladder (about 0.2 to 0.3 percent). This means that the potentiometer would have to be a thin-film device. To assure contact during each step of the staircase voltage generated by the ladder network, the mass-spring system of the potentiometer wiper has to be designed so that its resonant frequency is higher than the stepping rate of the counter. This way the wiper, even if it is vibrating, touches the substrate at least once during each step.

7. COST

Since no well-defined accuracy requirements for this timer exist and no mechanical configuration has been established in which this circuit has to fit, only a rough cost estimate can be made at this time. Prices for commercially available items in quantities of 1000 are as follows:

Item	Cost (each) (\$)
Binary ladder network, thin film, 10 bits $\pm 1/2$ LSB	13.00
Operational amplifier	0.55
Transistor array for voltage regulator and reset	0.90
Crystal 32,768 Hz (STATEK)	2.00

If the CMOS circuit is implemented on a UGA, the initial charge for the first 20 circuits is approximately \$20,000. After this, the cost per circuit (in quantities of 1000) is approximately \$25. The resistive material for the potentiometer will most likely be deposited on a part which serves another function. Therefore, it is not possible to estimate its cost without knowing the exact mechanical configuration. The unit cost for the first 1000 timers (less the potentiometer) assembled would be approximately \$50. For large volume applications, the UGA can be replaced by a custom circuit in which the comparator and regulator circuit can be incorporated. The production cost of this circuit should be in the range of \$5 to \$6. Crystals for high-acceleration application are not available as a stock item. Therefore, a cost estimate for a timer with a crystal oscillator able to survive more than 10,000 g can be worked out only for a specific case.

8. FUTURE WORK

To determine if the requirements for low power and short startup time can be met at higher frequencies, crystal oscillators in the frequency range from 1 to 6 MHz will be made on a breadboard with SOS dividers. Then some available crystals which have the potential of surviving a shock of more than 10,000 g will be tested.

The CMOS circuitry has to be redrawn in a way that uses only building blocks available in the UGA cell library. Thus, integration of the circuit can commence whenever there is a requirement.

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